UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,750	09/25/2003	Chad A. Cobbley	MICS:0078--1 (FLE/MAN) (0	1056

7590 06/01/2004

Michael G. Fletcher
Fletcher Yoder
P.O. Box 692289
Houston, TX 77269-2289

EXAMINER	
BLUM, DAVID S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/672,750	COBBLEY ET AL.	
	Examiner	Art Unit	
	David S Blum	2813	

-- The MAILING DATE of this communication app ars on the cover sheet with the c rrespondenc address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *35-39,45-49 and 63-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *35-39,45-49 and 63-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This action is in response to the amendment filed 9/25/03.

DETAILED ACTION

Claim Objections

1. Claims 38, 48, and 66 are objected to because of the following informalities: the claims recite that the "stack comprises a shingle stack". It is believed the applicant meant - - single stack - -. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 35, 37-39, 45, 47-49, 63, and 65-67 are rejected under 35 U.S.C. 102(e) as being anticipated by Pai (US006503776B2).

Pai teaches the device of claims 35, 37-39, 45, 47-49, 63, and 65-67 as follows.

Claim 35. An integrated circuit comprising:

a stack comprising at least two semiconductor die **(130 and 160, dummy chip 160 is of the sam material as the semiconductor chip, th r fore it is a**

semiconductor chip, column 3 lin s 19-20), each of the semiconductor die being coupled together by a first adhesive, the first adhesive **(166)** being curable at a first temperature; and

a substrate coupled **(substrate 120 coupled to stack through chip 110 and adhesive 162)** to one of the at least two semiconductor die by a second adhesive **(112)**, the second adhesive being curable at a second temperature lower than the first temperature. **(it is noted that Pai teaches this (column 3 lines 34-36). However, the steps of being curable at a first and second temperature are considered product by process limitations and are given no patentable weight.**
Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

Claim 37. The integrated circuit, as set forth in claim 35, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Claim 38. The integrated circuit, as set forth in claim 35, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(see figure 10, single stack)**.

Claim 39. The integrated circuit, as set forth in claim 35, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Claim 45. An integrated circuit comprising a stack of at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)**, each of the die being coupled to an adjacent die in the stack **(110)** by a respective layer of adhesive **(162)** prior to the stack being coupled to a packaging substrate. **(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight. Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)**

Claim 47. The integrated circuit, as set forth in claim 45, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Claim 48. The integrated circuit, as set forth in claim 45, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(See figur 10, single stack)**.

Claim 49. The integrated circuit, as set forth in claim 45, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Claim 63. An integrate circuit package comprising:

a substrate **(120)**; and

a die stack coupled to the substrate **(Figure 10)**, wherein the die stack comprises at least two semiconductor die **(130 and 160, dummy chip 160 is of the same material as the semiconductor chip, therefore it is a semiconductor chip, column 3 lines 19-20)** coupled together and wherein the dies stack is formed prior to being coupled to the substrate.

(The limitation of each die being coupled prior to the stack being coupled to a packaging substrate is considered a product by process limitation and given no patentable weight.

Even though product-by-process claims are limited by and defined by the process, determination of Patentability is based upon the product itself. The patenability of a product does not depend on its method of production." MPEP 2113)

Claim 65. The integrated circuit package, as set forth in claim 63, wherein the topside surface area of one of the at least two semiconductor die is less than the topside surface area of a second of the at least two semiconductor die **(See figure 10)**.

Claim 66. The integrated circuit package, as set forth in claim 63, wherein the stack of at least two semiconductor die is configured such that the stack comprises a shingle stack **(see figure 10, single stack)**.

Claim 67. The integrated circuit package, as set forth in claim 63, wherein at least one of the at least two semiconductor die comprises a memory die **(column 1 line 18)**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 36, 46, and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pai (US006503776B2) in view of Hakey (US006627477B1) or Moden (US006512303B2).

Pai teaches the device of claims 36, 46, and 64 as recited above in regard to claims 35, 45, and 63, except for explicitly teaching that the chips may be of different thickness.

(as the claims are identical, the rejection will not be repeated)

Claim 36. The integrated circuit, as set forth in claim 35, wherein one of the at least two semiconductor die is thicker than a second of the at least two semiconductor die.

Claim 46. The integrated circuit, as set forth in claim 45, wherein one of the at least two semiconductor die is thicker than a second of the at least two semiconductor die.

Claim 64. The integrated circuit package, as set forth in claim 63, wherein one of the at least two semiconductor die is thicker than a second of the at least two semiconductor die.

Pai teaches combining chips of processor, memory and associated logic into a single package (column 1 lines 17-19). Although not teaching that these chips may have a different thickness from each other, one skilled in the requisite art would know this. Hakey does not stack the die, but also connects die of logic chips and memory chips and teaches that these die have different thicknesses (column 2 lines 34-40), thus confirming that one would know that the chips of Pai could be of a different thickness from each other. Further, Moden teaches stacking and coupling chips having a different thickness (figure 4), thus it is known to stack chips (as Pai's stack) having a different thickness.

It would be obvious to one skilled in the requisite art at the time of the invention to modify Pai to include chips having a different thickness as suggest d by Pai's description of the chips, Hakey teaching that the chips listed by Pai have different

thickness s, and by Moden t aching that it is known to stack chips of different thicknesses.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David S. Blum whose telephone number is (757)-272-1687) and e-mail address is David.blum@USPTO.gov .

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached at (571)-272-1702. Our facsimile number all patent correspondence to be entered into an application is (703) 872-9306. The facsimile number for customer service is (703)-872-9317.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David S. Blum

May 27, 2004